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PATENT APPLICATION

ATTORNEY DOCKET NO. 10980422-3

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Jong Chan

Confirmation No.: 5386

Application No.: 09/846,868

Examiner: M. Maskulinski

Filing Date: May 1, 2001

Group Art Unit: 2113

Title: MEMORY CONTROLLER SUPPORTING REDUNDANT SYNCHRONOUS MEMORIES

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **March 23, 2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: **May 23, 2005**

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( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number_____ on _____

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Typed Name: **Patrick G. Billig**

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Respectfully submitted,

Jong Chan

By _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Jong Chan	Examiner:	Michael C. Maskulinski
Serial No.:	09/846,868	Group Art Unit:	2184
Filed:	May 1, 2001	Docket No.:	10980422-3
Title:	MEMORY CONTROLLER SUPPORTING REDUNDANT SYNCHRONOUS MEMORIES		

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed on March 23, 2005, appealing the final rejection of claims 37-48 of the above-identified application as set forth in the Final Office Action mailed November 24, 2004.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 50-0471 in the amount of $500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. § 41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 50-0471.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 37-48.

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed November 24, 2004, claims 37-48 were finally rejected. Claims 1-36 were canceled without prejudice in a preliminary amendment mailed to the Office on May 1, 2001. Claims 37-48 are pending in the application and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed November 24, 2004.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The subject matter of the independent claim involved in the Appeal is related to computer systems using a fault tolerant input/output (I/O) controller having redundant synchronous memories.

One aspect of the present invention, as claimed in independent claim 37, provides a method for controlling a transfer of data between a data processor (202) and a data unit (206). The method includes providing a plurality of control units (212), each control unit (212) having a capability to control the transfer of data between the data processor (202) and the data unit (206).

Each control unit (212) has a memory device (234) and signal paths (225, 266, 262, and 268) coupled to the memory device (234). The signal paths (225, 266, 262, and 268) enable access to the associated memory device (234). The method includes selecting one of the control units (212) as a master control unit (e.g., 212A) to control the transfer of data between the data processor (202) and the data unit (206). The method includes designating a second one of the control units (212) as a slave control unit (e.g., 212B). The method includes transferring the data between the data processor (202) and the data unit (206) by employing the memory device (e.g., 234A) in the master control unit (e.g., 212A), and synchronizing the memory device (e.g., 234A) in the master control unit (e.g., 212A) with the memory device (e.g., 234B) in the slave control unit (e.g., 212B). The synchronizing includes generating, in the master control unit (e.g., 212A), values for the signal paths (e.g., 225A, 266A, 262A, and 268A) associated with the master memory device (e.g., 234A) to transfer data to the master memory device (e.g., 234A), transferring a subset of the generated signal paths (e.g., 266A, 262A, and 268A) to the signal paths (e.g., 225B, 266B, 262B, and 268B) associated with the slave memory device (e.g., 234B), and allowing the generated signals to perform the data transfer to the master memory device (e.g., 234A) and the slave memory device (e.g., 234B). *See Specification*, at page 5, line 15 through page 7, line 2; at page 15, line 7 through page 17, line 26; at page 19, line 4 through page 21, line 8; and Figures 2, 3, 6, and 8.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether claims 37-46 are patentable under 35 U.S.C. § 102(b) over the McLaughlin et al. U.S. Patent No. 5,202,822.

II. Whether claims 47 and 48 are patentable under 35 U.S.C. § 103(a) over the combination of the McLaughlin et al. U.S. Patent No. 5,202,822 and the Kern et al. U.S. Patent No. 5,734,818.

ARGUMENT

I. The Applicable Law

With regard to a 35 U.S.C. § 102(b) anticipation rejection: "A person shall be entitled to a patent unless- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States." 35 U.S.C. § 102(b) (2004).

A rejection based on 35 U.S.C. § 102(b) can be overcome by: persuasively arguing that the claims are patentably distinguishable from the prior art; or, amending the claims to patentably distinguish over the prior art. M.P.E.P. § 706.02(b).

With regard to a 35 U.S.C. § 103 obviousness rejection: "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." M.P.E.P. 2141 (emphasis in the original). The Examiner bears the burden under 35 U.S.C. § 103 in establishing a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *In re Fine* at 1074. Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375, 379 (Fed. Cir. 1986). Third,

the reference or combined references must teach or suggest all of the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A. 1974).

The court in *Fine* stated:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."

In re Fine, 5 USPQ2d at 1599 (citations omitted).

There must be some teaching somewhere that provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem that it addresses. *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988); *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (C.C.P.A. 1979). In particular, "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based upon applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142 (emphasis added).

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). Furthermore, claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), *cert. denied*, 481 U.S. 1052 (1987). At the same time, a prior patent cited as a § 103 reference must be considered in its entirety, "*i.e.* as a *whole*, including portions that lead away from the invention." *Id.* That is, the Examiner must recognize and consider not only the similarities, but also the critical differences between the claimed invention and the prior art as one of the factual inquiries pertinent to any obviousness inquiry under 35 U.S.C. § 103. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990) (emphasis added). Finally, the Examiner must avoid hindsight. *Id.*

With regard for the test for obviousness under § 103, a statement that modifications of the prior art to meet the claimed invention would have been " 'well within the ordinary skill of the

art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993); M.P.E.P. § 2143.01 (emphasis in the original).

In conclusion, an applicant is entitled to a patent grant if any one of the elements of a *prima facie* case of obviousness is not established. The Federal Circuit has endorsed this view in stating: "If examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1448 (Fed. Cir. 1992).

II. Rejection of Claims 37-46 under 35 U.S.C. § 102(b) as being unpatentable over the McLaughlin et al. U.S. Patent No. 5,202,822.

Independent claim 37 is patentably distinct from the McLaughlin et al. Patent.

Claims 37-46 were rejected in a second Non-Final Office Action mailed May 26, 2004 over the McLaughlin et al. U.S. Patent No. 5,202,822. Independent claim 37 and claims 38-46 were distinguished over the McLaughlin et al. Patent in a Response mailed August 23, 2004. Independent claim 37 and claims 38-46 were again distinguished over the McLaughlin et al. Patent in a Response mailed January 24, 2005 in response to the Final Office Action mailed November 24, 2004.

In particular, the McLaughlin et al. Patent teaches a controller of a control system, which operates as a master, has a slave input/output processor (IOP) connected thereto which communicates with at least one device of a predetermined type, and a backup slave IOP connected thereto of the same type as the slave IOP, the slave IOP operating as a primary IOP to the device. A method for providing backup to the slave IOP by the backup slave IOP comprises the steps of loading the backup slave IOP with the same database as the slave IOP. The backup slave IOP eavesdrops on all communications from the controller to the slave IOP. When a write command is communicated to the slave IOP, the backup slave IOP taps the data from the bus and

updates the database. If the command is not a write command, it ignores the communication. (Abstract).

The McLaughlin et al. Patent includes a process control system 10 including a plant control network 11, in which a process controller 20 is operatively connected to the plant control network 11. The process controller 20 interfaces analog input and output signals, and digital input and output signals to process control system 10 from a variety of field devices that include valves, pressure switches, pressure gauges, thermocouples, etc. (Column 3, lines 22-38). The process controller 20 includes a controller A 30 and a controller B 40 which effectively operate as a primary and secondary controller. (Column 3, lines 60-64). A database maintained by the primary controller is communicated to the secondary controller via link 13. (Column 4, lines 30-32; Fig. 2). A track unit is coupled to local bus 93 of control unit 90 to implement the database transfer via link 13 to the other controller 30, 40 of the process controller 20. (Column 4, line 67 – column 5, line 3).

Controller A 30 interfaces to each I/O module 21 via a bus A 22, and controller B 40 interfaces to each I/O module 21 via a bus B 23. In addition, for redundancy purposes, controller A 30 is also connected to bus B 23 and controller B 40 is connected to bus A 22. (Column 4, lines 6-11). In I/O modules 21, signals on bus A 22 and bus B 23 are received by transceiver 201. Transceiver 201 communicates the signals to microcontroller 202. Microcontroller 202 communicates with EPROM 204 and RAM 205 through local bus 203. RAM 205 contains the information that forms the database for I/O module 21. (Column 5, lines 38-47; Fig. 4).

Synchronizing is a process whereby the same database is contained in both IOP(A) 21-A and IOP(B) 21-B. The information of the database of IOP(A) 21-A is requested by the controller 30 and then transferred to IOP(B) 21-B thereby causing the database of IOP(B) 21-B to be the same. (Column 8, lines 13-19). In normal operation, all write commands to IOP(A) 21-A from controller 30 are received by IOP(B) 21-B. IOP(B) 21-B eavesdrops on the communications. (Column 8, lines 28-31). IOP(B) 21-B eavesdrops on the communications by receiving all write commands from bus A 22.

Applicant submits that the McLaughlin et al. Patent does not teach or suggest the limitations of independent method claim 37 of synchronizing the memory device in the master

control unit with the memory device in the slave control unit, the synchronizing including: generating, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device; transferring a subset of the generated signal paths to the signal paths associated with the slave memory device; and allowing the generated signals to perform the data transfer to the master memory device and the slave memory device.

The Examiner states in the Response to Arguments section in the Final Office Action mailed November 24, 2004 that:

> in column 8, lines 28-33, McLaughlin et al. disclose that in normal operation, all transfers (i.e., writes) to the IOP(A) 21-A from controller are also received by IOP(B). IOP(B) eavesdrops on the communications since both IOP(A) and IOP(B) have a logical address of 1 in this example and the controller communicates to the IOPs by logical address. Further, in column 9, lines 60-65, McLaughlin et al. discloses that the read requests which were queued up by IOP(A) and not yet processed is known to the controller. The controller, then initiates to IOP(B) those read requests queued up at the time the failure of IOP(A) was detected. Thus, no communications (requests from other subsystems of system) go unanswered.

The synchronizing steps as recited in claim 37 are not taught or suggested by the McLaughlin et al. Patent. The eavesdropping cited by the Examiner is not the same as the synchronizing steps recited in claim 37. Claim 37 requires the master control unit *to generate, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device.* Example embodiments of such a master control unit and master memory device which can implement these steps of claim 37 include the master control unit 212A and master memory device 234A illustrated in Figure 6 of the present application. Memory controller 224A of master control unit 212A ensures that the data in master memory device 234A and slave memory device 234B is consistent. (See specification, page 9, lines 20-21). The signal paths associated with master memory device 234A include memory bus 230A. The signal paths associated with slave memory device 234B include memory bus 230B. Bus switches 290, 292, and 294 are used to exchange data between

the two memory buses 230A and 230B. (See specification, page 15, lines 7-21). Claim 37 requires master control unit 212A to generate values for signal paths 230A.

Claim 37 also requires *transferring a subset of the generated signal paths to signal paths associated with the slave memory device*. In one example implementation of the invention of claim 37, generated signal paths 230A associated with master memory device 234A are transferred to signal paths 230B associated with slave memory device 234B through bus switches 290, 292, and 294 of master control unit 212A and slave control unit 212 B.

In addition, claim 37 requires *allowing the generated signals to perform the data transfer to the master memory device and the slave memory device*. In one example implementation of the invention of claim 37, the signals generated in master control unit 212A perform the data transfer to master memory device 234A and slave memory device 234B through memory bus 230A and 230B, respectively.

In contrast, in the McLaughlin et al. Patent, IOP(A) 21-A and IOP(B) 21-B each individually receive signals for writing to their respective RAM memories 205 through bus A 22 or bus B 23 from controller A 30. There are no signals generated in slave IOP(A) 21-A that are transferred to backup slave IOP(B) 21-B. The signals provided to IOP(A) 21-A and IOP(B) 21-B are provided by controller A 30. Microcontroller 202 of each IOP 21 receives the signals from controller A 30 and can write data only to its own RAM 205 and not to the RAM of another IOP 21. In the method of claim 37, the slave control unit does not receive any signals from the data processor in the same manner as IOP(B) 21-B receives signals from controller A 30. In one example implementation of the invention of claim 37, slave memory device 234B is written by first memory controller 224A of master control unit 212A, not by second memory controller 224B of slave control unit 212B. The eavesdropping method described in the McLaughlin et al. Patent and cited by the Examiner provides a method for synchronization different than the method of synchronization recited in claim 37.

In summary, in the McLaughlin et al. Patent, synchronization is performed by controller A 30 communicating with microcontroller 202 of slave IOP(A) 21-A and

microcontroller 202 of backup slave IOP(B) 21-B. Microcontroller 202 of slave IOP(A) 21-A writes RAM 205 of IOP(A) 21-A, and microcontroller 202 of backup slave IOP(B) 21-B writes RAM 205 of IOP(B) 21-B to synchronize the memories. IOP(A) 21-A does not communicate with IOP(B) 21-B. In contrast, in the method of claim 37, the master control unit communicates with the slave control unit to perform the data transfer to the slave memory device to synchronize the memories.

In view of the above, Appellant respectfully assert that independent claim 37 is patentably distinct from the McLaughlin et al. Patent, and dependent claims 38-46 further define patentably distinct independent claim 37. Therefore, claims 37-46 are believed to be allowable. For the above reasons, Appellant respectfully requests the reversal of the Examiner's rejections to claims 37-46 under 35 U.S.C. § 102(b).

III. Rejection of Claims 47 and 48 under 35 U.S.C. § 103(a) as being unpatentable over the combination of the McLaughlin et al. U.S. Patent No. 5,202,822 and the Kern et al. U.S. Patent No. 5,734,818

The combination of the McLaughlin et al. Patent and the Kern et al. Patent fails to render claims 47 and 48 *prima facie* obvious.

Dependent claims 47 and 48 further define patentably distinct independent claim 37. Therfore, dependent claims 47 and 48 are also believed to be allowable. For the reasons detailed in Section II of the Argument above, Appellant respectfully requests the reversal of the Examiner's rejections to claims 47 and 48 under 35 U.S.C. § 103(a).

CONCLUSION

The claims of the pending application stand twice rejected. Independent claim 37 is pending in its original form and recites limitations that are not taught or suggested by the McLaughlin et al. Patent. For the above reasons, Appellant respectfully submits that the cited references neither anticipate nor render obvious claims of the present application. The pending claims distinguish over the cited references, and therefore, Appellant respectfully submits that the rejections must be withdrawn, and respectfully requests the Examiner be reversed and claims 37-48 be allowed.

Any inquiry regarding this Appeal Brief should be directed to either Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005 or David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 23 day of May, 2005.

By
Name: Patrick G. Billig

CLAIMS APPENDIX

1-36. (Cancelled)

37. (Previously Presented) A method for controlling a transfer of data between a data processor and a data unit, the method comprising:

providing a plurality of control units, each control unit having a capability to control the transfer of data between the data processor and the data unit, each control unit having a memory device and signal paths coupled to the memory device, the signal paths enabling access to the associated memory device;

selecting one of the control units as a master control unit to control the transfer of data between the data processor and the data unit;

designating a second one of the control units as a slave control unit;

transferring the data between the data processor and the data unit by employing the memory device in the master control unit; and

synchronizing the memory device in the master control unit with the memory device in the slave control unit, the synchronizing including:

generating, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device;

transferring a subset of the generated signal paths to the signal paths associated with the slave memory device; and

allowing the generated signals to perform the data transfer to the master memory device and the slave memory device.

38. (Previously Presented) The method of claim 37, wherein the generating step further comprises:

generating, in the master control unit, values for the signal paths associated with the slave memory device that enables access to the slave memory device.

39. (Previously Presented) The method of claim 37, further comprising:

associating an address and control signal path with each memory device that enables access to the corresponding memory device;

the generating step further comprising:

producing values for the address and control signal paths associated with the master memory device; and

the transferring step further comprising:

transmitting the address and control signal paths associated with the master memory device to the address and control signal paths associated with the slave memory device.

40. (Previously Presented) The method of claim 39, further comprising:

associating with the master memory device a first control signal that controls access to the slave memory device;

associating with each memory device a second control signal that controls access to the corresponding memory device;

the generating step further comprising:

producing values for the first control signal and the second control signal associated with the master memory device; and

the transferring step further comprising:

transmitting the first control signal associated with the master memory device to the second control signal associated with the slave memory device.

41. (Previously Presented) The method of claim 39, further comprising:

associating with each control unit a data signal path; and

the transferring step further comprising:

receiving data values for the data signal path associated with the master memory device; and

transmitting the received data values to the data signal path associated with the slave memory device.

42. (Previously Presented) The method of claim 37, further comprising:

associating with the signal paths associated with each memory device a control mechanism that enables a transfer of values from a first signal path to a second signal path; and

enabling the control mechanism associated with the master memory device and the control mechanism associated with the slave memory device to transfer values between the master signal paths and the slave signal paths.

43. (Previously Presented) The method of 42, further comprising:

disabling the control mechanism associated with a memory device to inhibit a transfer and receipt of signal paths values.

44. (Previously Presented) The method of claim 37, further comprising:

suspending the master control unit from controlling the data transfer between the data processor and the data unit;

enabling the slave control unit to control the transfer of data between the data processor and the data unit; and

transferring the data between the data processor and the data unit by employing the memory device in the slave control unit.

45. (Previously Presented) The method of claim 44, wherein the suspending step further comprises:

determining that the master control unit has experienced an operational failure.

46. (Previously Presented) The method of claim 45, wherein the determining step further comprises:

receiving an indication that the memory device in the master control unit has failed.

47. (Previously Presented) The method of claim 37, further comprising:

disabling the master control unit from accessing the slave memory device; and

suspending operation of the slave control unit.

48. (Previously Presented) The method of claim 47, wherein the disabling step further comprises:

determining that the slave control unit has experienced an operational failure.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None